REMARKS

Claims 1, 3-26 are pending in this application. Claims 2 and 8-18 have been canceled and claims 19-26 have been newly added. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment, which is captioned "Version with Markings to Show Changes Made."

Rejections under 35 USC §102(b) and §103(a)

Claims 1 and 7 stand rejected under 35 USC §102(b) as being anticipated by Uglow et al (U.S. Patent No. 6,251,770). Also, Claims 2 stand rejected under 35 USC §103(a) as unpatentable over Uglow et al in view of Chung et al (U.S. Patent No. 6,184,142).

Applicants respectfully traverse these rejections.

There are two methods for forming a dual damascene wiring. One method is first forming a trench, and then forming a via hole, as explained in Uglow et al. The other is first forming a via hole, and then forming a wiring trench as employed in the applicant's invention.

The conventional method of first forming a via hole and then forming a wiring trench is illustrated in Figs. 11A to 12E of the present drawings. When a via hole is first formed, a problem arises as described in the present specification at pages 10-14, referring to Figs. 12A-16D. Namely, abnormal etching occurs as a result of the etching of a shoulder formed by the bottom of the wiring trench and the side wall of the via hole (see specification, page 11, line 17 to page 12, line 1).

When the trench etching is done on a structure already formed with a via hole, etching can occur also from the side surface of the via hole. Such etching produces the shoulder portion at an upper portion of the via (contact) hole. When a via hole is etched after a trench is etched, there occurs no such shoulder etching because the via is etched in a flat bottom surface of the trench.

Claims 1-7 are directed to solving the problem of shoulder etching unique to the method of first forming a via hole, and then forming a wiring trench. The Examiner referred to Fig. 10B of Uglow et al, which discloses a dielectric material layer 104' forming of TEOS or FSG which shows a large etching selectively compared to the barrier layer 102', and a low K dielectric material layer 106'. A wiring trench is formed in the low K dielectric material layer 106'. A via hole is formed from the bottom surface of the wiring trench to the conducting region 120 through the remaining thickness of the low K dielectric material layer 106', the dielectric material layer 104', and the barrier layer 102'. Abnormal etching does not occur in this case.

Claim 1 has been further amended to incorporate the limitations of claim 2. Some additional amendments have been made to clarify that the via hole runs from the bottom surface of the wiring trench to the underlying conductive region, and the shoulder of the via hole is etched to some extent.

The Examiner referred to Fig. 3G of Chung et al regarding claim 2. Fig. 3G of Chung et al shows a wiring trench having slanted side walls, and a straight via hole. The slanted side walls are shown to connect the edges of the hard mask layers 14 and 18.

In Chung et al, however, there is no bottom surface of the wiring trench at a first depth, nor is there a contact hole having an upper portion whose cross-sectional area gradually increases toward an upper

level and reaches to bottom surface of the wiring trench. In Chung et al, two hard mask layer 18 and 14 are patterned, and the dual damascene structure is etched in one process. There is no description why the slanted side surfaces are formed. It may be considered that low K material layer 13 is thick, and the etching condition is selected to produce a slanted side-wall. Uglow discloses first forming a wiring trench, and then forming a via hole from the bottom of the wiring trench to the underlying conducting region as illustrated in Fig. 10B. There is shown no etch stopper layer at the bottom of the wiring trench.

For at least these reasons, claim 1, as amended, patentably distinguishes over Uglow et al and Chung et al. Claim 7, depending from claim 1, also patentably distinguishes over Uglow et al and Chung et al for at least the same reasons.

Therefore, the 35 USC §102(b) rejection and the 35 USC §103(a) rejection should be withdrawn.

Claims 3, 5 and 6 stand rejected under 35 U.S.C. §103(a) as being obvious over Uglow et al in view of Tsai et al (U.S. Patent No. 6,319,814 B1).

Applicants respectfully traverse this rejection.

First, Tsai et al does not remedy the deficiencies of Uglow et al discussed above.

Moreover, the Examiner referred to the etch stop layer 206, an undoped oxide layer 208, and FSG layer 210. These disclosure does not teach or suggest the limitations of claim 3. Claim 3 of the present application recites an etch stopper layer, a third kind of the insulating layer, a second kind of the insulating layer, and a first kind of the insulating layer, stacked in this order on a surface of the underlie. If the

undoped oxide layer 208 is taken as the third kind of the insulating layer, there is only one layer thereon. There can be found no separate second and first kinds of the insulating layers.

For at least these reasons, claim 3 patentably distinguishes over Uglow et al and Tsai et al. Claims 5 and 6, depending from claim 3 also patentably distinguishes over Uglow et al and Tsai et al for at least the same reasons.

Therefore, the 35 USC §103(a) rejection should be withdrawn.

Claim 4 stands rejected under 35 U.S.C. §103(a) as being obvious over Uglow et al in view of Tsai et al and further in view of Chung et al.

Applicants respectfully traverse this rejection.

As discussed above, the slanted surface of Chung et al is a side wall, or side-wall/bottom of the wiring trench. Chung et al discloses no separate bottom surface of the wiring trench and shoulder portion of the via hole.

It should again be noted that the present invention is directed to solving the problem caused in first forming a via hole, and then forming a wiring trench. The cited references do not disclose the problem occurring in this process and suggest no solution to this problem resulting in the recitations of claim 4.

For at least these reasons, claim 4 patentably distinguishes over Uglow et al, Tsai et al and Chung et al.

Therefore, the 35 USC §103(a) rejection should be withdrawn.

New Claims

Claims 19-26 have been added. These new claims are supported by the disclosure in the specification. Specifically, Claim 19 is supported in the specification at page 16, lines 19-24 and Figs. 1B and 2B. Claim 20 is supported in the specification at page 17, lines 12-15. Claim 21 is supported in the specification in Fig. 2B. Claim 22 is supported in Figs. 1B and 2B. Claim 23 is supported in Figs. 1B and 2B. Claim 24 is supported in the specification at page 21, line 23 to page 22, line 3. Claim 25 is supported in the specification at page 19, lines 20-24. Claim 26 is supported in the specification at page 15, lines 2-7.

Additional amendments has been made to the drawing and the claims to correct various informalities. Figs. 1A-1F and Fig. 2A-2F were inadvertently mislabeled. Description on page 15, line 2-7 refers the film 13 and the layer 14, which cannot be found in Fig. 1A, but are shown in Fig. 2A. On the other hand, description on page 19, line 25 to page 20, line 1 refers to the film 56 in Fig. 2A, which cannot be found in Fig. 2A, but is shown in Fig. 1A.

Figs. 17AA-17BD and 18AA-18BD are used in the description of the embodiments, but are labeled inadvertently as PRIOR ART. The legends prior art in these figures have been deleted. Also, the description in the Brief Description of the Drawings has been corrected.

In view of the aforementioned amendments and accompanying remarks, all pending claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: Version with Markings to Show Changes Made
Request for Approval of Drawing Corrections w/Figs. 1, 2, 17 & 18 marked in red ink

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VERSION WITH MARKINGS TO SHOW CHANGES MADE S.N. 09/735,479

IN THE CLAIMS:

Claims 2 and 8-18 have been canceled.

Claims 19-26 have been added.

Claims 1 and 4 have been amended as follows:

1. (Amended) A semiconductor device comprising:

an underlie having a conductive region in a surface layer of said underlie;

an insulating etch stopper film covering a surface of said underlie;

an interlayer insulating film formed on said insulating etch stopper film;

a wiring trench formed in said interlayer insulating film, said wiring trench having a bottom surface at a first depth from a surface of said interlayer insulating film, and a side wall;

a contact hole extending from a said bottom surface of said wiring trench to a surface of the conductive region through a remaining thickness of said interlayer insulating film and through said insulating etch stopper film; and

a dual damascene wiring layer embedded in said wiring trench and in said contact hole,

wherein said interlayer insulating film includes a first kind of an insulating layer surrounding a side wall and the bottom surface of said wiring trench and a second kind of an insulating layer disposed under the first kind of the insulating layer and having etching characteristics different from the first kind of the insulating layer, and

wherein said contact hole has an upper portion whose cross sectional area gradually increases toward an upper level and reaches the bottom surface of said wiring trench in the first kind of the insulating layer.

4. (Amended) A semiconductor device according to claim 3, wherein said contact hole has a portion whose cross sectional area gradually increases from an intermediate level of the second kind of the insulating layer toward an upper level and reaches the bottom surface of said wiring trench.